REMARKS

Rejection Under 35 U.S.C. §112

Claims 13, 14, 27 and 28 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In Regards to Claims 13, 14, 27 and 28, applicant has amended claims 13, 27 and 28 to clarify the claims. Applicant believes the amendments now make the Examiner's rejections under 35 U.S.C. §112 moot. Accordingly, Applicant respectfully requests the withdrawal of the rejections of Claims 13, 14, 27 and 28 under 35 U.S.C. §112.

Rejection Under 35 U.S.C. §102(b)

Claims 10-12, 15-17, 20, 23, 24 and 29 were rejected under 35 U.S.C. §102(b) as being anticipated by Chang et al. (U.S. Patent 5,792,681).

CLAIM 10

In Regards to Claim 10, Applicant has amended Claim 10 to clarify limitations that patentably distinguish the present application from the Chang et al. reference. In particular, the Chang et al reference does not disclose or teach depositing a nitride layer "wherein the nitride layer is in contact with the oxide layer and all of the exposed surface areas created by the patterning of the oxide layer" as is disclosed and now claimed in Claim 10 of the present application. Therefore, Claim 10 is patentably distinguishable form the Chang et al. reference.

Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 10 under 35 U.S.C. §102(b) and the allowance of Claim 10. Moreover, since Claims 11-14 further define and depend from Claim 10, Applicant asserts that Claims 11-14 are also patentably distinct from the cited reference and respectfully requests their allowance.

Claim 12

In regards to Claim 12, Examiner Pham has asserted that the Chang et al. reference discloses using a nitride layer in at least one isolation island as a capacitor dielectric in forming a capacitor. However, Applicant respectfully asserts, the Change et al. reference does not disclose or teach the limitation of using the nitride layer "in at least one of the isolation islands" as is disclosed and claimed in Claim 12 of the present application. Moreover, the Chang et al. reference does not disclose or teach using the nitride layer "as a capacitor dielectric" as is disclosed and claimed in Claim 12 of the present application. Referring to the Chang et al. reference, the dielectric of the capacitor disclosed is composed of a layer of oxide11 that is said to be 55 to 75 A thick (column 4, lines 27-31) plus a nitride layer 14 that is said to be 270-300A thick (column 4, lines 41-46). The Chang et al. reference further goes on to teach that the purpose of the nitride layer 14 is to protect the oxide layer 11 in forming the capacitor region (Column 4, lines 46-58). Therefore, the Chang et al. reference, teaches away from using a single nitride layer for a capacitor dielectric as is disclosed and claimed in Claim 12 of the present application.

Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 10 under 35 U.S.C. §102(b) and the allowance of Claim 12.

Claim 15

In regards to Claim 15, Applicant has amended Claim 15 to clarify limitations that patentably distinguish the present application from the Chang et al. reference. In particular, the Chang et al reference does not disclose or teach depositing a dielectric layer "wherein the dielectric layer is in contact with the oxide layer and all the exposed surface areas created by the patterning of the oxide layer." With reference to the argument for Claim12, nor does the Chang et al reference disclose or teach "using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming the capacitor" as is disclosed and claimed in Claim 15 of the present application. As provided above, Claim 15 is patentably distinguishable from the Chang et al. reference.

Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 15 under 35 U.S.C. §102(b) and the allowance of Claim 10. Moreover, since Claims 16-22 further define and depend from Claim 15, Applicant asserts that Claims 16-22 are also patentably distinct from the cited reference and respectfully requests their allowance.

Claim 16

In regards to Claim 16, with reference to the argument regarding Claim 12, the Chang et al. reference teaches away from a capacitor dielectric of a single layer of silicon nitride as is disclosed and claimed in Claim 16 of the present application.

Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 16 under 35 U.S.C. §102(b) and the allowance of Claim 16.

Claim 23

In regards to Claim 23, Applicant has amended Claim 23 to clarify limitations that patentably distinguish the present application from the Chang et al. reference. In particular, the Chang et al reference does not disclose or teach forming a dielectric layer "wherein the dielectric layer is in contact with the oxide layer and all the exposed surface areas created by the patterning of the oxide layer." With reference to the argument for Claim 12, nor does the Chang et al reference disclose or teach "using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming the capacitor" as is disclosed and claimed in Claim 23 of the present application. As provided above, Claim 23 is patentably distinguishable from the Chang et al. reference.

Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 23 under 35 U.S.C. §102(b) and the allowance of Claim 10. Moreover, since Claims 24-32 further define and depend from Claim 15, Applicant asserts that Claims 24-32 are also patentably distinct from the cited reference and respectfully requests their allowance.

Rejection Under 35 U.S.C. §102(e)

Claims 1-5, 8, and 9 were rejected under 35 U.S.C. §102(e) as being anticipated by Liaw (U.S. Patent 6,258,678).

Claim 1

In regards to Claim 1, the Liaw reference does not disclose or teach the method of "forming anisotropic contact openings that extend through the layer of dielectric and the layer of oxide using a dry etch with a single mask" as is disclosed and claimed in Claim 1 of the present application. The Liaw reference discloses and teaches a method of forming self aligned contact openings that includes several dry and wet etches (Figures 4 –8 and Column 4, Line 52 through Column 5, Line 62). In particular, referring to Figures 4 and 5, Column 4, Line 53 through Column 5, Line 22, an anisotropic REI procedure is first used to create an opening through an interlevel dielectric layer (12). Next, a first wet etch is used to remove polymer residue (Column 5, lines 24-30) followed by a second dry etch to remove the thin nitride layer (11) (Column 5, lines 37-40). The process is completed with a second wet etch to remove the thin silicon oxide layer 8 (Column 5, lines 45-46). As discussed above, the Liaw reference teaches away from "forming anisotropic contact openings that extend through the layer of dielectric and the layer of oxide using a dry etch with a single mask" as is disclosed and claimed in Claim 1 of the present application. Therefore, Claim 1 is Patentably distinct from the Liaw reference.

Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 1 under 35 U.S.C. §102(e) and the allowance of Claim 1. Moreover, since Claims 2-9 further define and depend from Claim 1, Applicant asserts that Claims 2-9 are also patentably distinct from the cited reference and respectfully requests their allowance.

Rejection Under 35 U.S.C. §103(a)

Claims 25 and 26 were rejected under 37 C.F.R. §103(a) as being unpatentable over Chang et al. (U.S. Patent 5,792,681).

Claims 25 and 26

In Regards to Claims 25 and 26, the Chang et al. Reference does not teach or suggest alone or in combination the use of open tube deposition and a dopant source of phosphorus oxychloride as is disclosed and claimed respectively in Claims 25 and 26 of the present application. Therefore, Claims 25 and 26 are patentably distinct from the Chang et al. Reference.

Allowable Subject Matter

In regards to Claims 33-37, Applicant acknowledges and thanks Examiner Pham for their allowance.

In regards to Claims 18, 19, 21, 22, and 30-32, Applicant acknowledges they were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION

Claims 10, 13, 15, 23, 27, 28 are amended. Claims 5 and 7 are withdrawn from consideration. Claims 33-37 have been allowed. Claims 1 –37 are pending in this application. Applicant respectfully submits that the claims are now in condition for allowance and notification to that effect is earnestly requested. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2206.

If necessary, please charge and additional fees or credit overpayment to Deposit Account No. 501373.

Respectfully submitted,

Date: 9-3-02

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MARKED UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS

10. (Amended Once) A method of forming an integrated circuit, the method comprising:

forming an oxide layer on a surface of a substrate, the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device;

patterning the oxide layer to expose predetermined areas of the surface of the substrate;

depositing a nitride layer overlaying the oxide layer and the exposed surface areas of the substrate, wherein the nitride layer is in contact with the oxide layer and all of the exposed surface areas created by the patterning of the oxide layer; and

implanting ions through the nitride layer, wherein the nitride layer is an implant screen for the implanted ions.

13. (Amended Once) The method of claim 10, further comprising:

performing a dry etch to form anisotropic contact openings that extend through the layer of nitride and through the layer of oxide to access selected device regions formed in the substrate by the implanted ions.

15. (Amended Once) A method of forming an integrated circuit, the method comprising:

forming an oxide layer on a surface of a substrate, the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device of the integrated circuit;

patterning the oxide layer to expose predetermined areas of the surface of the substrate;

depositing a dielectric layer overlaying the oxide layer and the exposed surface areas of the substrate, wherein the dielectric layer has a higher dielectric constant than a dielectric constant of the oxide layer, further wherein the dielectric layer is in contact with the oxide layer and all of the exposed surface areas created by the patterning of the oxide layer;

implanting ions through the dielectric layer;

diffusing the ions to form device regions in selected isolation islands in the substrate; and

using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor.

23. (Amended Once) A method of forming an integrated circuit, the method comprising:

forming a first oxide layer on a surface of a substrate, the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device of the integrated circuit;

patterning the first oxide layer to expose predetermined areas of the surface of the substrate;

implanting and diffusing ions into the substrate to form device regions;

forming a dielectric layer overlaying the oxide layer and the exposed areas of the surface of the substrate, wherein the dielectric layer has a dielectric constant higher than a dielectric constant of the oxide layer, further wherein the dielectric layer is in contact with the oxide layer and all of the exposed surface areas created by the patterning of the oxide layer; and

using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor.

27. (Amended Once) The method of claim 25, wherein a non-selective etch is used to expose the surface of the [semiconductor] substrate adjacent device regions before the dielectric layer is formed.

28. (Amended Once) The method of claim [25] 27, wherein the non-selective etch uses [etchant used is] a wet etchant containing hydrogen fluoride.

2814

First Named Inventor	James D. Beasom
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TRANSMITTAL
FORM UNDER
37 CFR 1.10

(LARGE ENTITY)

Title: INTEGRATED CIRCUIT WITH MOS CAPACITOR

Commissioner for Patents
Box Non-Fee Amendment
Washington, DC 20231

Enclosures

The following documents are enclosed:

X Amendment and Response under 37 C.F.R. §1.111 (11 pgs.).
X A return postcard.

Please charge any additional fees or credit any overpayments to Deposit Account No. 501373.

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I certify that this correspondence and the identified documents are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Box Non-Fee Amendment, Washington, D. C. 20231 on September 3, 2002.

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